

**REMARKS**

Upon entering this amendment, claims 1-13 and 15-22 will be pending in the current Application. Claims 5, 9, 12, and 13 have been amended; claim 14 has been cancelled; and claims 21 and 22 have been added. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

The Examiner states that the title of the invention is not descriptive; however, Applicants respectfully disagree. The current title, "Processing System Having Sequential Address Indicator Signal" is descriptive and clearly indicative of the invention to which the claims are directed. For example, each of the above independent claims is related to generating or providing one, two, or three different sequence signals which provide indications of address sequence. Therefore, Applicants submit that the current title need not be amended.

**Claim Objections**

The Examiner objected to claims 5, 9, 11, and 12. Applicants have amended claims 5, 9, and 12 to address all of the Examiner's objections. Note that the claim objection made in paragraph 5 of the current Office Action relates to claim 11; however, Applicants believe that this objection was intended for claim 12 since the language the Examiner points to is found in claim 11 and not claim 12. Therefore, Applicants have amended claim 12 to take care of this objection, too. Applicants submit that all claim objections have been resolved.

Claim Rejections under 35 U.S.C. 103(a)*Claims 1 – 2 and 21*

Applicants respectfully submit that claims 1 and 2 are patentable over US Patent No. 6,275,926 (hereinafter referred to as Samra) and US Patent No. 5,594,765 (hereinafter referred to as Oh). With respect to claim 1, Applicants submit that Samra and Oh, alone or in combination, do not teach or suggest each and every element of claim 1. For example, claim 1 includes means for generating a second sequence signal that when negated indicates that the current address is not sequential to the previous address. That is, the second sequence signal is generated to provide an indication that the current address is in fact not sequential to the previous address. This is not taught or suggested by Samra or Oh. The Examiner states that Oh's "seq\_int#" signal, "which specifies either sequential or non-sequential (interleaved) burst mode," teaches this. However, Applicants respectfully disagree. The seq\_int# signal, as described in col. 3, lines 16-21, when asserted indicates a sequential counting scheme to be used in generating an address and when negated, indicates an interleaved count scheme to be used. However, simply because it indicates an interleaved count scheme does not guarantee that the addresses are non-sequential. For example, referring to the table in col. 6 and lines 5-28 of col. 6, there are many interleaved sequences which are actually fully sequential (such as the first and last entries of the table). Furthermore, even while seq\_int# is negated to indicate interleaved modes, in most of the interleaving examples provided in the table, there are addresses which are sequential. During these sequential sections, the seq\_int# is not again asserted because it is still in interleaved mode, and furthermore, asserting it for these sections would destroy the functionality of Oh. Therefore, the negation of the seq\_int# does not necessarily indicate that two addresses are not sequential. At most, it indicates that they may not be sequential.

Furthermore, the negation of the seq\_int# signal indicates that the counting scheme *will be* interleaved, thus providing an indication of the relation of a subsequent address to a current address but provides no indication of the relation of a current address to a previous one. That is, the seq\_int# does not indicate a relation of the current address to a previous one because it is a forward looking signal. Also, one would not be motivated to modify the seq\_int# of Oh to do so.

because the purpose of seq\_int# is to ensure that the counter generates the appropriate address and is not used to indicate whether each current address is not sequential to the previous one. Therefore, Oh does not teach or suggest a signal that is generated to definitely indicate that the current address is not sequential to the previous address, as claimed in claim 1. For at least these reasons, the Examiner has failed to make a *prima facie* case of obviousness.

Claims 2-3 have not been independently addressed because they depend directly or indirectly from allowable claim 1 and are therefore also allowable for at least those reasons provided above with respect to claim 1.

### *Claims 3 - 9*

Applicants respectfully submit that claims 3-9 are patentable over Samra in view of Oh. With respect to claim 3, Applicants submit that Samra and Oh, alone or in combination, do not teach or suggest each and every element of claim 3. Firstly, claim 3 includes a fetch unit which generates first, second, and third sequence signals. Neither Samra nor Oh illustrate a fetch unit which generates first and second sequence signals. The Examiner agrees that Samra does not teach a fetch unit, but says that Oh teaches generating a first sequence signal because of Oh's LATCH signal. However, the signals of Oh, such as the LATCH signal, are not generated by a fetch unit. The signals of Oh cited by the Examiner are provided *as inputs* to a counter to properly control a burst access. However, they are not generated by a fetch unit. Furthermore, claim 3 requires generating a second sequence signal that when negated indicates that the current address is not sequential to the previous address. The Examiner again cites the seq\_int# signal of Oh. However, as was described above in reference to claim 1, the seq\_int# signal of Oh does not definitely indicate that the current address is not sequential to the previous address, as claimed in claim 3. That is, as described above, when seq\_int# is negated, it simply indicates that the addresses may not be sequential because the counter is no longer operating in a sequential mode. For example, it may indicate an interleaving mode which, as discussed above, may be sequential or may include sequential portions. Furthermore, as also described above, the negation of the seq\_int# signal indicates that the counting scheme *will be* interleaved, thus providing an indication of the relation of a subsequent address to a current address but provides no indication of the relation of a current address to a previous one. Therefore, many of the reasons provided

above with respect to claim 1 also apply with respect to claim 3, and for at least these reasons, Applicants submit that claim 3 is allowable over Samra in view of Oh.

Claims 4-9 have not been independently addressed because they depend directly or indirectly from allowable claim 3 and are therefore also allowable for at least those reasons provided above with respect to claim 3.

*Claims 10-12*

Applicants respectfully submit that claims 10-12 are patentable over US Patent No. 6,151,662 (hereinafter referred to as Christie) in view of Oh. With respect to claim 10, Applicants submit that Christie and Oh, alone or in combination, do not teach each and every element of claim 10. For example, claim 10 claims an address bus for providing a current address, a previous address, and a data address wherein the data address occurs before the current address and after the previous address. That is, claim 10 requires an intervening data address between the current and previous addresses. Furthermore, claim 10 claims a fetch unit for generating a first sequence signal that when asserted indicates that the current address is sequential to the previous address and when negated indicates that the current address may not be sequential to the previous address. Neither Christie, Oh, nor their combination teach or suggest these elements.

The claimed first sequence signal, for example, can indicate whether the current address is sequential to the previous address even when there is an intervening data address. Therefore, even if a burst is interrupted with a data access (either to another device or the same device), the first sequence may be used to continue its previous burst mode access. The Examiner agrees that Christie has not taught a fetch unit for generating the first sequence signal. The Examiner therefore states that the seq\_int# signal of Oh teaches the first sequence signal as claimed in claim 10. However, Applicants respectfully disagree. Firstly, the seq\_int# is not generated by a fetch unit. Secondly, the seq\_int# signal is used as an input to a counter so that, when asserted, the counter knows to count sequentially within a burst access. However, it is not asserted to indicate that a current address is sequential to the previous address when a data address occurs between the current and previous address. Oh also does not discuss burst counter 2 with respect to an interruption of a burst access with a data address. Therefore, one would not be motivated

to modify any of the signals of Oh to provide the same information as the claimed first sequence signal. Furthermore, once the seq\_int# is asserted, it indicates the counting scheme *to be* employed. That is, it indicates that the subsequent address will be sequential to the current one, and does not provide any indication of the relation of a previous address (which, in this claim, is also *prior to an intervening data address*) to a current address. Therefore, for at least these reasons, Applicants submit that claim 10 is allowable over Christie in view of Oh.

Claims 11-12 have not been independently addressed because they depend directly or indirectly from allowable claim 10 and are therefore also allowable for at least those reasons provided above with respect to claim 10.

*Claims 13-17 and 22*

Applicants respectfully submit that claims 13-17 and 22 are patentable over Samra in view of Oh. With respect to claim 13, Applicants submit that Samra and Oh, alone or in combination, do not teach or suggest each and every element of claim 13. For example, claim 13 claims a fetch unit for providing a second sequence signal which indicates if the current address is sequential to the previous address. The Examiner agrees that Samra does not teach a fetch unit for providing a second sequence signal as claimed in claim 13. However, the Examiner states that the seq\_int# signal of Oh teaches the claimed second sequence signal. Applicants respectfully disagree. As described above, the seq\_int# is used as an input to a counter so that, when asserted, the counter knows to count sequentially during a burst access. That is, it only indicates what counting scheme is to be employed, thus providing an indication of the sequentiality of a subsequent address to a current one. However, it provides no indication of the relation of a previous address to a current address. That is, the seq\_int# does not indicate whether the current address is sequential to the previous address because the seq\_int# signal is a forward looking signal. Therefore, for at least these reasons, Applicants submit that claim 13 is allowable over Samra in view of Oh.

Furthermore, claim 22 has been added to further define the first and second sequence signals. Claim 22 depends off of claim 14 which further indicates that the first sequence signal indicates that the current address may not be sequential to the previous address prior to the second sequence signal indicating that the current address is not sequential to the previous

address. Claim 22 further defines that the second sequence signal is provided in response to resolving a branch condition code. None of the cited reference teach these limitations either. Therefore, claims 14-17 and 22 have not all been independently addressed because they are allowable over the cited references for at least those reasons provided above with respect to claim 13.

*Claims 18-20*

Applicants respectfully submit that claims 18-20 are patentable over Christie in view of Oh. With respect to claim 18, Applicants submit that Christie and Oh, alone or in combination, do not teach each and every element of claim 18. For example, claim 18 claims a fetch unit for providing a first sequence signal that indicates if a current instruction address is sequential to a previous instruction address even if a data address is provided between the current instruction address and the previous instruction address. Neither Christie, Oh, nor their combination teach or suggest these elements.

The claimed first sequence signal, for example, can indicate whether the current address is sequential to the previous address even when there is an intervening data address. Therefore, even if a burst is interrupted with a data access (either to another device or the same device), the first sequence may be used to continue its previous burst mode access. The Examiner states that Christie teaches the first sequence signal as claimed in claim 18 due to the branch prediction taught by Christie. However, Applicants respectfully disagree. The Examiner states that a signal which indicates whether a branch was mispredicted teaches the first sequence signal. However, a branch misprediction signal only indicates whether a branch was mispredicted. The Examiner states that "where the branch was predicted not-taken, this third [sic] signal would indicate that the current instruction address is not sequential to the previous instruction address." (Applicants assume the Examiner meant to talk about the first signal.) Firstly, this branch misprediction signal does not indicate if a current instruction address actually is sequential to a previous instruction address. For example, if a branch were mispredicted, then a new address (either the branch target address or the address that would have been sequential after the mispredicted branch instruction) would have to be fetched to remedy the misprediction, where the branch misprediction signal cannot be relied upon to indicate that the current instruction address is in

fact sequential to a previous instruction address. This new address could either be sequential or non-sequential with respect to the previous instruction address. Also, the branch misprediction address only indicates whether a branch was mispredicted so that, for example, the pipeline can be flushed. But again, this signal cannot be used to indicate the actual sequentiality or non-sequentiality of a current address to a previous address.

Furthermore, the branch misprediction signal does not address the issue of intervening data addresses. For example, in a sequential fetch of instruction addresses (regardless of whether these instructions are branches or not), there may be an intervening data address, where the claimed first sequence signal indicates if the current instruction address is sequential to a previous instruction address even if an intervening data address is provided. The branch misprediction signal discussed by the Examiner does not even address this situation because it is only used for branch prediction and may therefore be irrelevant in this situation. Furthermore, none of the other signals in the cited reference (such as the LATCH or seq\_int# of Oh teach or suggest the first sequence signal as claimed in claim 18). Therefore, for at least these reasons, Applicants submit that claim 18 is allowable over the cited references.

Claims 18-20 have not been independently addressed because they depend directly or indirectly from allowable claim 18 and are therefore also allowable for at least those reasons provided above with respect to claim 18.

**Conclusion**

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action, yet reserve the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

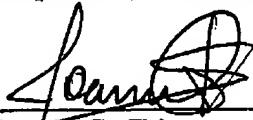
If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 502117.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Motorola, Inc.  
Law Department

Customer Number: 23125

By: 

Joanna G. Chiu  
Attorney of Record  
Reg. No.: 43,629  
Telephone: (512) 996-6839  
Fax No.: (512) 996-6854

RECEIVED  
CENTRAL FAX CENTER

OCT 24 2003

OFFICIAL